Notice of References Cited	Application/Control No. 09/888,474	Applicant(s)/Patent Under Reexamination AMATANGELO ET AL.	
	Examiner Ayal I Sharon	Art Unit 2123	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-6,272,668	08-2001	Teene, Andres R.	716/10
	B	US-5,180,937	01-1993	Laird et al.	327/276
	C	US-6,286,126	09-2001	Raghavan et al.	716/6
	D	US-6,430,731	08-2002	Lee et al.	716/6
	E	US-6,442,741	08-2002	Schultz, Richard T.	716/6
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Pouya, B. et al. "Modifying User-Defined Logic for Test Access to EMbedded Cores". Proc, Int'l Test Conf. 1997. Nov. 1-6, 1997. pp.60-68.
	V	Munch, M et al. "Automating RT-Level Operand Isolation to Minimize Power Consumption in Datapaths". Proc. of COnf. on Design, AUtomation, Test in Europe. 2000. pp.624-633.
	W	Touba, N.A. et al. "Testing Embedded Cores Using Partial Isolation Rings". 15th IEEE VLSI Test Symposium. May 1, 1997. pp.10-16.
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.